May 1999

National Semiconductor

LM6162
High Speed Operational Amplifier

General Description

The LM6162 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/µs and 100 MHz gain-bandwidth product (stable for gains as low as +2 or −1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

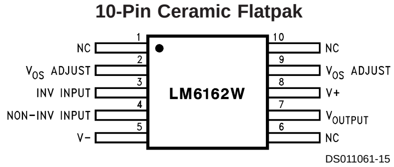
- High slew rate: 300 V/µs
- High gain-bandwidth product: 100 MHz
- Low supply current: 5 mA
- Fast settling time: 120 ns to 0.1%
- Low differential gain: <0.1%
- Low differential phase: <0.1˚
- Wide supply range: 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

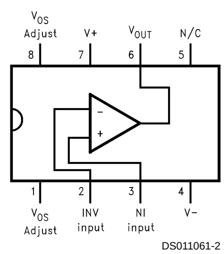
- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

Connection Diagrams

10-Pin Ceramic Flatpak



Top View
See NS Package Number W10A



See NS Package Number N08E or J08A

Temperature Range			Package	NSC Drawing
Military $-55˚C \leq T_A \leq +125˚C$	**Industrial** $-25˚C \leq T_A \leq +85˚C$	**Commercial** $0˚C \leq T_A \leq +70˚C$		
LM6162N			8-Pin Molded DIP	N08E
LM6162J/883 5962-9216501PA			8-Pin Ceramic DIP	J08A
LM6162WG/883 5962-9216501XA			10-Lead Ceramic SOIC	WG10A

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Connection Diagrams (Continued)

Temperature Range			Package	NSC Drawing
Military $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	**Industrial** $-25^{\circ}C \leq T_A \leq +85^{\circ}C$	**Commercial** $0^{\circ}C \leq T_A \leq +70^{\circ}C$		
LM6162W/883 5962-9216501HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V^+–V^-)	36V
Differential Input Voltage (Note 2)	±8V
Common-Mode Input Voltage (Note 3)	(V^+−0.7V) to (V^- + 0.7V)
Output Short Circuit to GND (Note 4)	Continuous
Soldering Information	
Dual-In-Line Package (N)	
Soldering (10 seconds)	260˚C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215˚C
Infrared (15 seconds)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Storage Temperature Range	−65˚C ≤ T_J ≤ +150˚C
Max Junction Temperature	150˚C
ESD Tolerance (Note 5)	±1100V

Operating Ratings

Temperature Range (Note 6)	
LM6162	−55˚C ≤ T_J ≤ +125˚C
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and R_L ≥ 100 kΩ, unless otherwise specified. Limits in standard typeface are for T_A = T_J = 25˚C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	Units
V_{OS}	Input Offset Voltage		±3	±5 **±8**	mV max
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Average Drift		7		µV/˚C
I_{bias}	Input Bias Current		2.2	3 **6**	µA max
I_{OS}	Input Offset Current		±150	±350 **±800**	nA max
$\frac{\Delta I_{OS}}{\Delta Temp}$	Input Offset Current Average Drift		0.3		nA/˚C
R_{IN}	Input Resistance	Differential	180		kΩ
C_{IN}	Input Capacitance		2.0		pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 9)	1400	1000 **500**	V/V min
		R_L = 10 kΩ	6500		V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	V min
			−13.2	−12.9 **−12.7**	V max
		Supply = +5V (Note 10)	4.0	3.9 **3.8**	V min
			1.6	1.8 **2.0**	V max
CMRR	Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	100	83 **79**	dB min
PSRR	Power Supply Rejection Ratio	±10V ≤ V_S ≤ ±16V	93	83 **79**	dB min

DC Electrical Characteristics (Continued)

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq$ 100 kΩ, unless otherwise specified. Limits in standard typeface are for $T_A = T_J$ = 25˚C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	Units
V_O	Output Voltage Swing	Supply = ±15V, R_L = 2 kΩ	+14.2	+13.5 **+13.3**	V min
			−13.4	−13.0 **−12.7**	V max
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 10)	4.2	3.5 **3.3**	V min
			1.3	1.7 **2.0**	V max
I_{OSC}	Output Short Circuit Current	Sourcing	65	30 **20**	mA min
		Sinking	65	30 **20**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	mA max

AC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, $R_L \geq$ 100 kΩ, and $C_L \leq$ 5 pF, unless otherwise specified. Limits in standard typeface are for $T_A = T_J$ = 25˚C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	Units
GBW	Gain-Bandwidth Product	f = 20 MHz	100	80 **55**	MHz min
		Supply = ±5V	70		MHz
SR	Slew Rate	A_V = +2 (Note 11)	300	200 **180**	V/µs min
		Supply = ±5V	200		V/µs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5		MHz
t_s	Settling Time	10V step, to 0.1% A_V = −1, R_L = 2 kΩ	100		ns
ϕ_m	Phase Margin	A_V = +2	45		deg
	Differential Gain	NTSC, A_V = +2	<0.1		%
	Differential Phase	NTSC, A_V = +2	<0.1		deg
e_n	Input Noise Voltage	f = 10 kHz	10		nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.2		pA/√Hz

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 3: a) In addition, the voltage between the V^+ pin and either input pin must not exceed 36V.

b) When the voltage applied to an input pin is driven more than 3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20 mA to limit damage from self-heating.

Note 4: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 5: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100 pF in series with 1500Ω.

Note 6: The typical thermal resistance, junction-to-ambient, of the molded plastic DIP (N package) is 105˚C/W. For the molded plastic SO (M package), use 155˚C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 7: Typical values are for T_J = 25˚C, and represent the most likely parametric norm.

Note 8: Limits are guaranteed, by testing or correlation.

AC Electrical Characteristics (Continued)

Note 9: Voltage Gain is the total output swing (20V) divided by the magnitude of the input signal required to produce that swing.

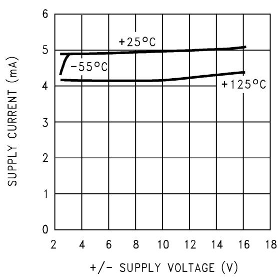
Note 10: For single-supply operation, the following conditions apply: $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$. Pin 1 and Pin 8 (V_{OS} Adjust pins) are each connected to pin 4 (V^-) to realize maximum output swing. This connection will increase the offset voltage.

Note 11: $V_{IN} = 10V$ step. For ±5V supplies, $V_{IN} = 1V$ step.

Note 12: A military RETS electrical test specification is available on request.

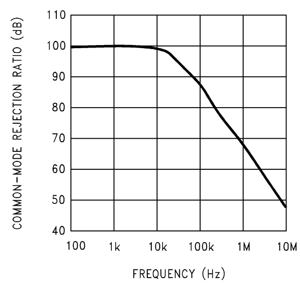
Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25^\circ C$ unless otherwise noted

Supply Current vs Supply Voltage



DS011061-16

Common-Mode Rejection Ratio



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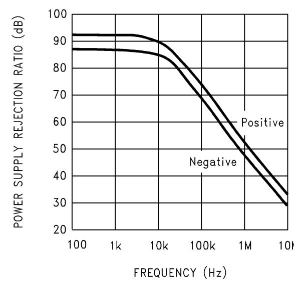
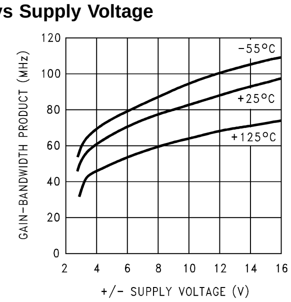
Power Supply Rejection Ratio



DS011061-18

Gain-Bandwidth Product vs Supply Voltage



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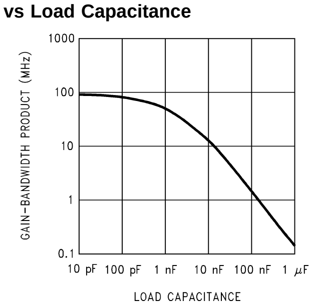
Gain-Bandwidth Product vs Load Capacitance



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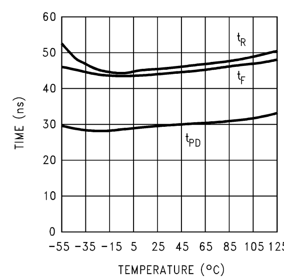
Propagation Delay, Rise and Fall Times



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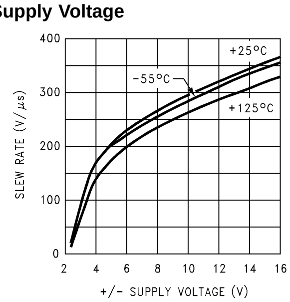
Slew Rate vs Supply Voltage



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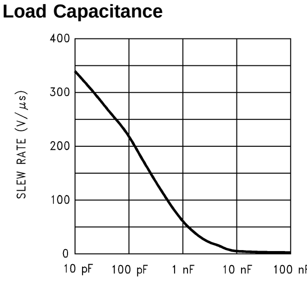
Slew Rate vs Load Capacitance



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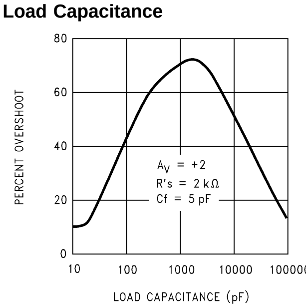
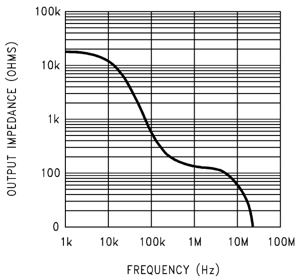
Overshoot vs Load Capacitance



DS011061-24

Typical Performance Characteristics R_L = 10 kΩ, T_A = 25˚C unless otherwise noted (Continued)

Output Impedance (Open-Loop)



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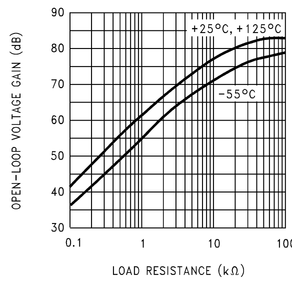
Voltage Gain vs Load Resistance



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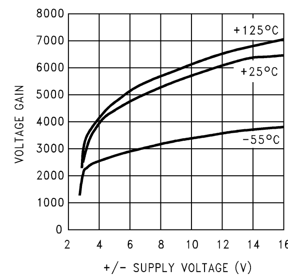
Voltage Gain vs Supply Voltage



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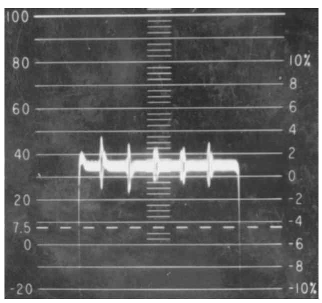
Differential Gain (Note)

Differential Gain (Note 13)



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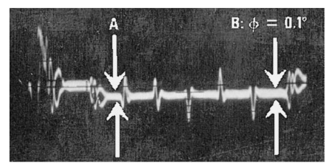
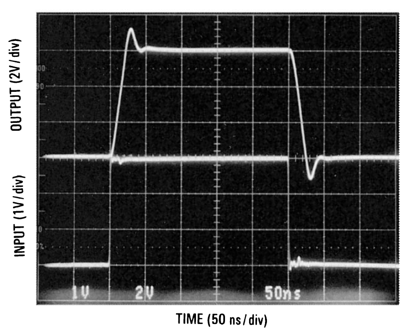
Differential Phase (Note 13)



DS011061-5

Note 13: Differential gain and differential phase measured for four series LM6162 op amps configured with gain of +2 each, in series with a 1:16 attenuator and an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

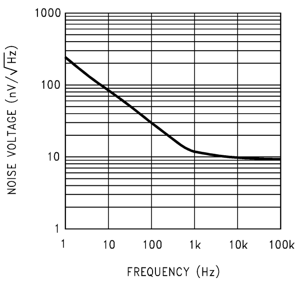
Step Response; Av = +2



DS011061-6

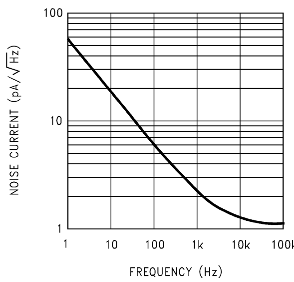
Typical Performance Characteristics R_L = 10 kΩ, T_A = 25˚C unless otherwise noted (Continued)

Input Noise Voltage



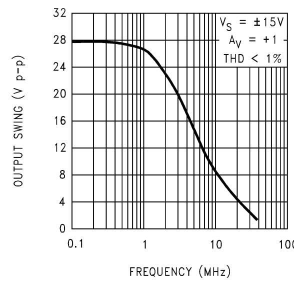
DS011061-28

Input Noise Current



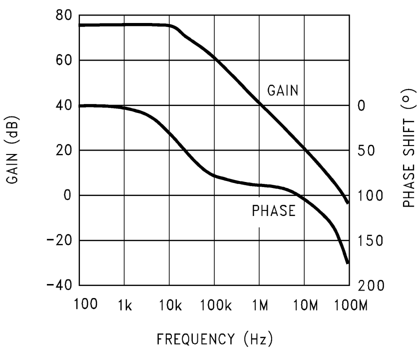
DS011061-29

Power Bandwidth



DS011061-30

Open-Loop Frequency Response



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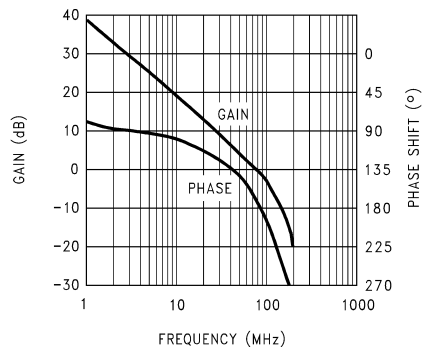
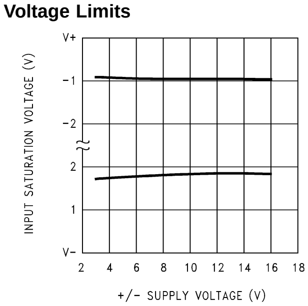
Open-Loop High-Frequency Response



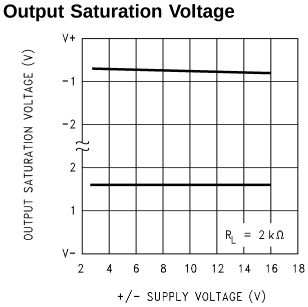
DS011061-9

Common-Mode Input Voltage Limits



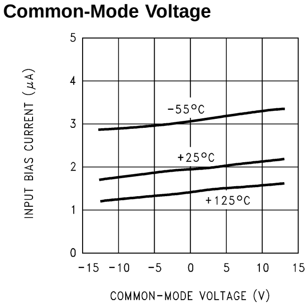
DS011061-31

Output Saturation Voltage



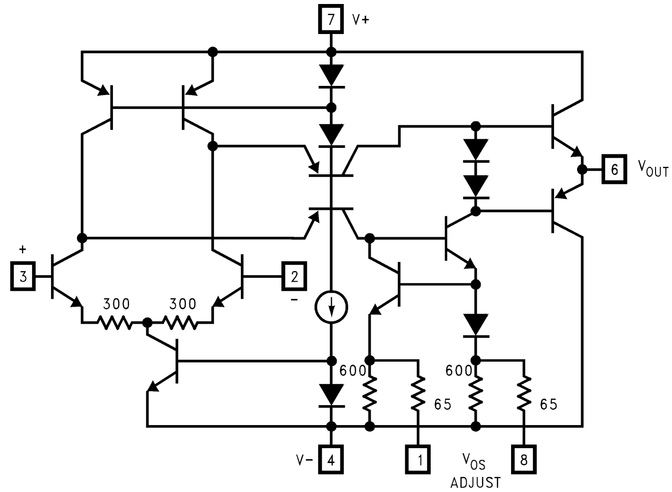
DS011061-32

Bias Current vs Common-Mode Voltage



DS011061-33

Simplified Schematic



DS011061-1

Application Tips

The LM6162 has been decompensated for a wider gain-bandwidth product than the LM6361. However, the LM6162 still offers stability at gains of 2 (and −1) or greater over the specified ranges of temperature, power supply voltage, and load. Since this decompensation involved reducing the emitter-degeneration resistors in the op amp's input stage, the DC precision has been increased in the form of lower offset voltage and higher open-loop gain.

Other op amps in this family include the LM6361, LM6364, and LM6365. If unity-gain stability is required, the LM6361 should be used. The LM6364 has been decompensated for operation at gains of 5 or more, with corresponding greater gain-bandwidth product (125 MHz, typical) and DC precision. The fully-uncompensated LM6365 offers gain-bandwidth product of 725 MHz, typical, and is stable for gains of 25 or more. All parts in this family, regardless of compensation, have the same high slew rate of 300 V/µs (typ).

The LM6162 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6162 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing may occur in low-gain circuits with large capacitive loads.

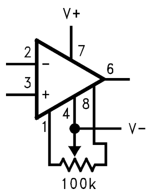
Power supply bypassing is not as critical for LM6162 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LM6162, and is recommended for every design. 0.01 µF to 0.1 µF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 µF to 10 µF of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit frequency response. At low gains (+2 or −1), a feedback capacitor C_f from output to inverting input will compensate for the phase lag caused by capacitance at the inverting input. Typically, values from 2 pF to 5 pF work well; however, best results can be obtained by observing the amplifier pulse response and optimizing C_f for the particular layout.

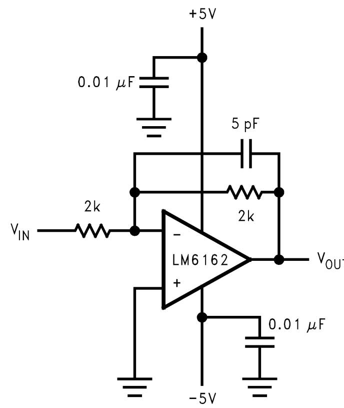
Typical Applications

Offset Voltage Adjustment



DS011061-11

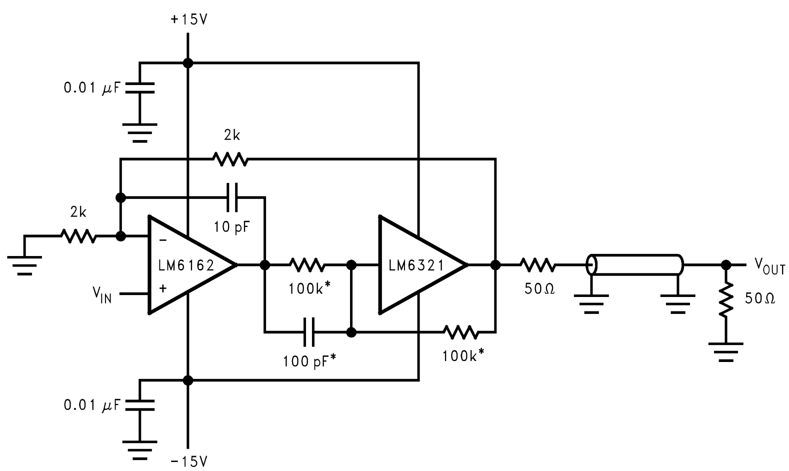
Inverting Amplifier, 30 MHz Bandwidth



DS011061-12

Operation on ±15V supplies results in wider bandwidth, 50 MHz (typ).

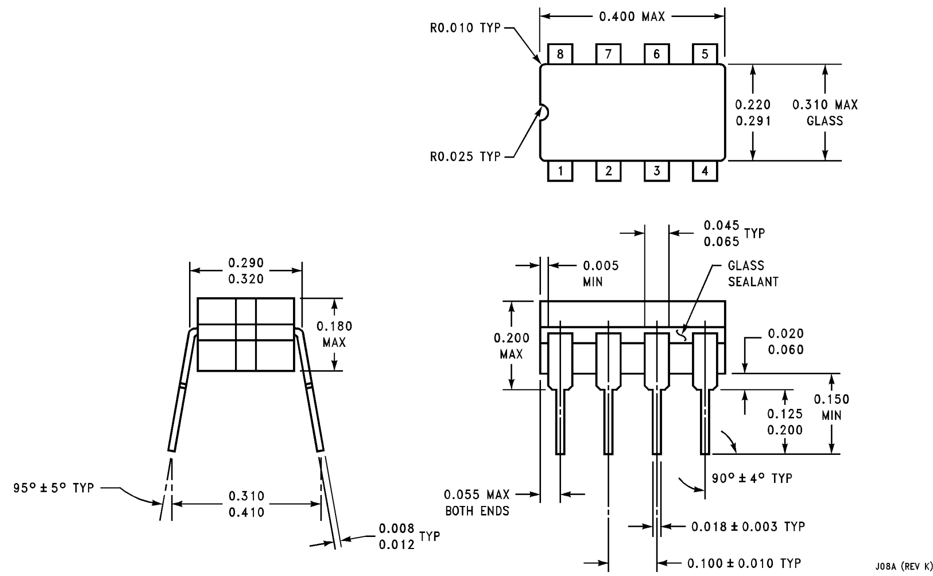
Video Cable Driver



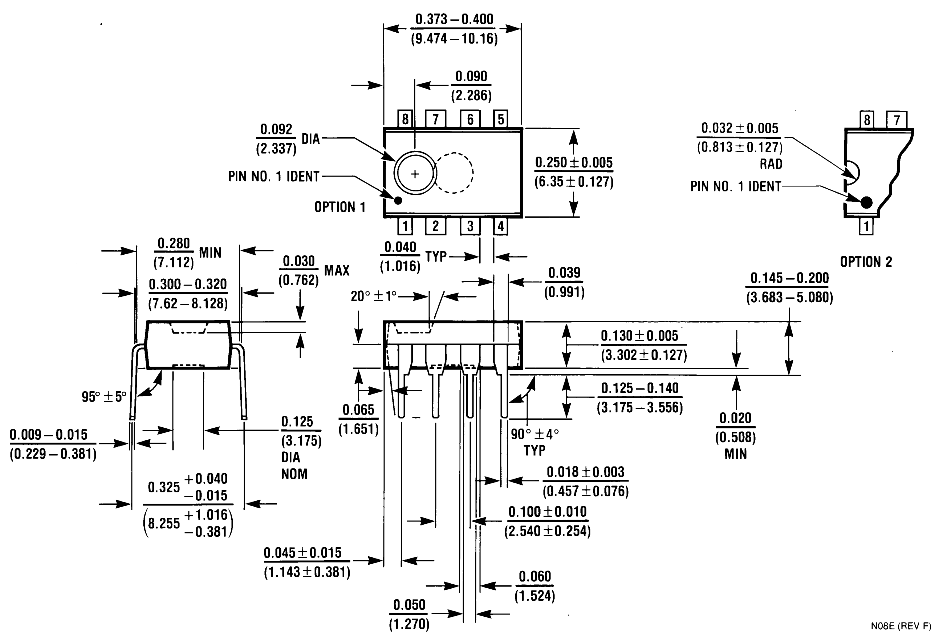
DS011061-13

* Network required when operating on supply voltage over ±5V, for overvoltage protection of LM6321. If ±5V supplies are used, omit network and connect output of LM6162 directly to input of LM6321.

Physical Dimensions inches (millimeters) unless otherwise noted

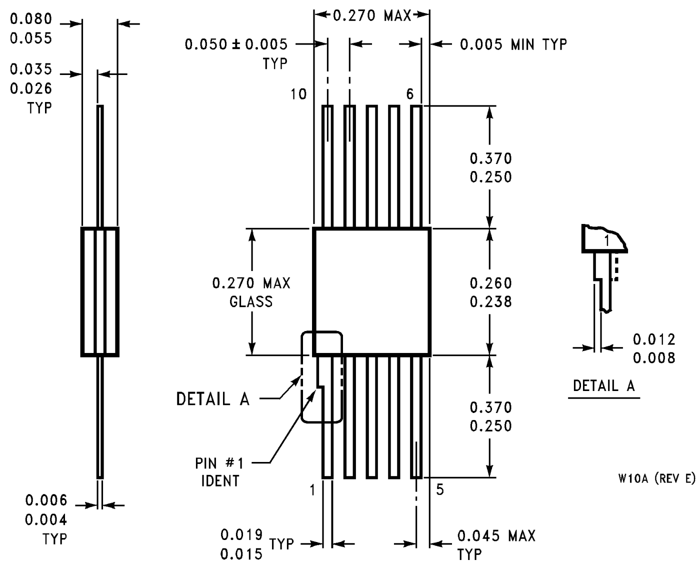


Ceramic Dual-In-Line Package (J)
Order Number LM6162J/883
NS Package Number J08A



Molded Dual-In-Line Package (N)
Order Number LM6162N
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



10-Pin Ceramic Flatpak
Order Number LM6162W/883
NS Package Number W10A

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